UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P O Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

77541 7590 12/08/2008

Maryam Imam and LSI Corporation
95 South Market Street
Suite 570
San Jose, CA 95113

EXAMINER	
LEE, CHUN KUAN	
ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 12/08/2008

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,521	02/09/2004	Sam Nemazie	SILICONSTOR-02US	1050

TITLE OF INVENTION: SWITCHING SERIAL ADVANCED TECHNOLOGY ATTACHMENT (SATA) TO A PARALLEL INTERFACE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$755	$0	$0	$755	03/09/2009

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

77541 7590 12/08/2008

Maryam Imam and LSI Corporation
95 South Market Street
Suite 570
San Jose, CA 95113

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)

(Signature)

(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,521	02/09/2004	Sam Nemazie	SILICONSTOR-02US	1050

TITLE OF INVENTION: SWITCHING SERIAL ADVANCED TECHNOLOGY ATTACHMENT (SATA) TO A PARALLEL INTERFACE

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	YES	$755	$0	$0	$755	03/09/2009

EXAMINER	ART UNIT	CLASS-SUBCLASS
LEE, CHUN KUAN	2181	710-074000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

☐ Issue Fee

☐ Publication Fee (No small entity discount permitted)

☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

☐ A check is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P O Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/775,521	02/09/2004	Sam Nemazie	SILICONSTOR-02US	1050

77541 7590 12/08/2008

Maryam Imam and LSI Corporation
95 South Market Street
Suite 570
San Jose, CA 95113

EXAMINER	
LEE, CHUN KUAN	
ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 12/08/2008

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 308 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 308 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

Notice of Allowability	Application No.	Applicant(s)	
	10/775,521	NEMAZIE, SAM	
	Examiner	Art Unit	
	Chun-Kuan Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *09/23/2008*.

2. ☒ The allowed claim(s) is/are *1,5-19,23-32 and 36-45*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 5/9/08 & 9/15/08
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Alford W. Kindred/
Supervisory Patent Examiner, Art Unit 2181

DETAILED ACTION

I. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

1. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated May 09, 2008 and September 15, 2008 are acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

II. EXAMINER'S AMENDMENTS

OPTIONS AVAILABLE TO THE APPLICANT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by **37 CFR § 1.312**. To ensure consideration of such an amendment, it **MUST** be submitted no later than the payment of the issue fee.

AUTHORIZATION FOR THE CORRECTIONS BY THE EXAMINER

3. Authorization for this examiner's amendment was given in a telephone interview with Attorney Maryam Imam, having Reg. No. 38,190, on December 4, 2008. Accordingly, since a complete record of the interview has been incorporated in the instant examiner's amendment, no separate interview summary form is included in the instant office letter **MPEP § 713.04**.

CORRECTIONS MADE IN THE APPLICATION

4. The application has been amended as following:

IN THE CLAIMS:

The below described amendments to the claims are necessary to further clarify the claimed invention.

NOTE: The claims amended by this examiner's amendment have been referred to by their original claim number.

5. In claim 1, "... A switch coupled between a plurality of host units and a device for communicating therebetween and comprising:

a) a first serial advanced technology attachment SATA port coupled to a first host unit and including a first host task file, said first port for causing access, to the device, by the first host unit, the first host task file responsive to commands sent by the first host unit;

b) a second SATA port coupled to a second host unit and including a second host task file, said second port for causing access to the device, by the second host unit, the second host task file responsive to commands sent by the second host unit;

c) a third parallel ATA port including a device task file, coupled to a device, for causing access to the device, by the first or second host units, the device configured to support command queuing and operative to generate an original queue depth value

indicative of the number of commands that the device can queue from either of the first or second host units; and

d) an arbitration and control circuit, coupled to said first host task file and said second host task file and said device task file for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state, the arbitration and control circuit being responsive to the original queue depth value and operative to alter the original queue depth value to be a queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that the total number of commands that can be queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less than that which it is thereby preventing commands being lost by an overrun of the original queue depth value by either of the first or second host units ..." should be replaced with

-... A switch coupled between a plurality of host units and a device for communicating therebetween and comprising:

a) a first serial advanced technology attachment (SATA) port coupled to a first host unit and including a first host task file, said first port for accessing, to the device, by the first host unit, the first host task file responsive to commands sent by the first host unit;

b) a second SATA port coupled to a second host unit and including a second host task file, said second port for accessing to the device, by the second host unit, the second host task file responsive to commands sent by the second host unit;

c) a third parallel ATA (PATA) port including a device task file, coupled to the device, for accessing the device, by the first or second host units, the device supports queuing of the commands sent by the first and second host units and generates an original queue depth value indicative of a number of commands that the device can queue from either of the first or second host units; and

d) an arbitration and control circuit, coupled to said first host task file, said second host task file, and said device task file for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting the commands from either of the first or second host units, at any given time, including when the device is not in an idle state, the arbitration and control circuit being responsive to the original queue depth value and alters the original queue depth value to be a new queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that a total number of commands queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less than the original queue depth value thereby preventing the commands sent by the first and second host units from being lost by an overrun of the original queue depth value by either of the first or second host units ...-.

6. In claim 5, line 1, "... recited in claim 4 ..." should be replaced with -... recited in claim 1 ...-.

7. In claim 8, line 2, "... causes concurrent access ..." should be replaced with -... causes the concurrent access ...-.

8. In claim 9, line 1, "... in the form of data ..." should be replaced with -... in form of data ...-.

9. In claim 12, line 1, "... in the form of data ..." should be replaced with -... in form of data ...-.

10. In claim 14, line 3, "... for identifying a host ..." should be replaced with -... for identifying either the first or second host unit ...-.

11. In claim 17, line 2, "... (FIS) first-in-first-out (FIFO) ..." should be replaced with -... (FIS) first-in-first-out (FIFO) circuit ...-.

12. In claim 18, "... A switch comprising:

a first serial advanced technology attachment (SATA) port for connection to a first host unit, the first port including a first host task file responsive to commands sent by the first host unit;

a second SATA port for connection to a second host unit, the second port including a second host task file responsive to commands sent by the second host unit;

a third parallel ATA port for connection to a device, the third port including a device task file, the device configured to support command queuing and operative to generate an original queue depth value indicative of the number of commands that the device can queue from either of the first or second host units; and

an arbitration and control circuit coupled to said first host task file and said second host task file and said device task file, for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state, the arbitration and control circuit being responsive to the original queue depth value and operative to alter the original queue depth value to be a queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that the total number of commands that can be queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less than that which it is thereby preventing

commands being lost by an overrun of the original queue depth value by either of the first or second host units ..." should be replaced with

-... A switch comprising:

a first serial advanced technology attachment (SATA) port for connection to a first host unit, the first port including a first host task file responsive to commands sent by the first host unit;

a second SATA port for connection to a second host unit, the second port including a second host task file responsive to commands sent by the second host unit;

a third parallel ATA (PATA) port for connection to a device, the third PATA port including a device task file, the device supports queuing of the commands sent by the first and second host units and generates an original queue depth value indicative of a number of commands that the device can queue from either of the first or second host units; and

an arbitration and control circuit coupled to said first host task file and said second host task file and said device task file, for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting the commands from either of the first or second host units, at any given time, including when the device is not in an idle state, the arbitration and control circuit being responsive to the original queue depth value and alters the original queue depth value to be a new queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that a total number of commands that

can be queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less than the original queue depth value thereby preventing the commands sent by the first and second host units from being lost by an overrun of the original queue depth value by either of the first or second host units ...-.

13. In claim 25, line 2, "... concurrent access ..." should be replaced with -... the concurrent access ...-.

14. In claim 26, line 1, "... in the form of data ..." should be replaced with -... in form of data ...-.

15. In claim 29, line 1, "... in the form of data ..." should be replaced with -... in form of data ...-.

16. In claim 31, "... A switch that is connectable to a first host unit, a second host unit and a device via serial advanced technology attachment (SATA) links, said switch comprising:

a first SATA port for connection to a first host unit, the first port including a first host task file responsive to commands sent by the first host unit;

a second SATA port for connection to a second host unit, the second port including a second host task file responsive to commands sent by the second host unit;

a third parallel ATA port for connection to a device, the third port including a device task file, the device configured to support command queuing and operative to generate an original queue depth value indicative of the number of commands that the device can queue from either of the first or second host units; and

an arbitration and control circuit, coupled to said first host task file and to said second host task file and said device task file, for selecting one of the first or second host units to concurrently access the device through the switch, by accepting commands, from either of the first or second host units, at any given time, including when the device is not in an idle state, the arbitration and control circuit being responsive to the original queue depth value and operative to alter the original queue depth value to be a queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that the total number of commands that can be queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less than that which it is thereby preventing commands being lost by an overrun of the original queue depth value by either of the first or second host units ..." should be replaced with

-... A switch that is connectable to a first host unit, a second host unit and a device via serial advanced technology attachment (SATA) links, said switch comprising:

a first SATA port for connection to the first host unit, the first SATA port including a first host task file responsive to commands sent by the first host unit;

a second SATA port for connection to the second host unit, the second SATA port including a second host task file responsive to commands sent by the second host unit;

a third parallel ATA (PATA) port for connection to the device, the third PATA port including a device task file, the device supports queuing of the commands sent by the first and second host units and generates an original queue depth value indicative of a number of commands that the device can queue from either of the first or second host units; and

an arbitration and control circuit, coupled to said first host task file, to said second host task file, and to said device task file, for selecting one of the first or second host units to concurrently access the device through the switch, by accepting the commands from either of the first or second host units, at any given time, including when the device is not in an idle state, the arbitration and control circuit being responsive to the original queue depth value and alters the original queue depth value to be a new queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that a total number of commands queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less than the original queue depth value thereby preventing the commands sent by the first and second host units from being lost by an overrun of the original queue depth value by either of the first or second host units ...-.

17. In claim 38, line 2, "... concurrent access ..." should be replaced with -... the concurrent access ...-.

18. In claim 39, line 1, "... in the form of data ..." should be replaced with -... in form of data ...-.

19. In claim 42, line 1, "... in the form of data ..." should be replaced with -... in form of data ...-.

20. In claim 44, line 1, "... the queue depth value ..." should be replaced with -... the new queue depth value ...-.

21. In claim 45, lines 4-5, "... with a queue depth value that is no more than one-half that reported by the device ..." should be replaced with -... with the new queue depth value that is no more than one-half of the original queue depth value that was reported by the device ...-.

III. DISTINGUISHING FEATURES RECITED IN THE CLAIMS

ALLOWABLE SUBJECT MATTER

22. Claims 1, 5-19, 23-32 and 36-45 are allowed.

The following is an **Examiner's Statement of Reasons for Allowance**, **See MPEP 1302.14**:

23. The primary reason for allowance of claim 1 in the instant application is the combination with the inclusion in the claim that there are "**... A switch coupled between a plurality of host units and a device for communicating therebetween and comprising:**

a) a first serial advanced technology attachment (SATA) port coupled to a first host unit and including a first host task file, said first port for accessing, to the device, by the first host unit, the first host task file responsive to commands sent by the first host unit;

b) a second SATA port coupled to a second host unit and including a second host task file, said second port for accessing to the device, by the second host unit, the second host task file responsive to commands sent by the second host unit;

c) a third parallel ATA (PATA) port including a device task file, coupled to the device, for accessing the device, by the first or second host units, the device supports queuing of the commands sent by the first and second host units and generates an original queue depth value indicative of a number of commands that the device can queue from either of the first or second host units; and

d) an arbitration and control circuit, coupled to said first host task file, said second host task file, and said device task file for selecting one of the first host

or second host units to concurrently access the device, through the switch, by accepting the commands from either of the first or second host units, at any given time, including when the device is not in an idle state, the arbitration and control circuit being responsive to the original queue depth value and alters the original queue depth value to be a new queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that a total number of commands queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less than the original queue depth value thereby preventing the commands sent by the first and second host units from being lost by an overrun of the original queue depth value by either of the first or second host units ..." The prior art of record including the disclosures of Grieff et al. (US Patent 6,961,813), "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya et al. (US Pub.: 2003/0131166), Ooi et al. (US Patent 6,854,045) and Ooi et al. (US Patent 6,961,787) neither anticipates nor renders obvious the above recited combination. Because claims 5-17 and 44-45 depend directly or indirectly on claim 1, these claims are considered allowable for at least the same reasons noted above.

24. The primary reason for allowance of claim 18 in the instant application is the combination with the inclusion in the claim that there are "**... A switch comprising:**

a first serial advanced technology attachment (SATA) port for connection to a first host unit, the first port including a first host task file responsive to commands sent by the first host unit;

a second SATA port for connection to a second host unit, the second port including a second host task file responsive to commands sent by the second host unit;

a third parallel ATA (PATA) port for connection to a device, the third PATA port including a device task file, the device supports queuing of the commands sent by the first and second host units and generates an original queue depth value indicative of a number of commands that the device can queue from either of the first or second host units; and

an arbitration and control circuit coupled to said first host task file and said second host task file and said device task file, for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting the commands from either of the first or second host units, at any given time, including when the device is not in an idle state, the arbitration and control circuit being responsive to the original queue depth value and alters the original queue depth value to be a new queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that a total number of commands that can be queued by the first and second host units remains the same as the original queue depth value

thereby misrepresenting the original queue depth value to the first and second host units to be less than the original queue depth value thereby preventing the commands sent by the first and second host units from being lost by an overrun of the original queue depth value by either of the first or second host units ..." The prior art of record including the disclosures of Grieff et al. (US Patent 6,961,813), "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya et al. (US Pub.: 2003/0131166), Ooi et al. (US Patent 6,854,045) and Ooi et al. (US Patent 6,961,787) neither anticipates nor renders obvious the above recited combination. Because claims 19 and 23-29 depend directly or indirectly on claim 18, these claims are considered allowable for at least the same reasons noted above.

25. The primary reason for allowance of claim 31 in the instant application is the combination with the inclusion in the claim that there are "**... A switch that is connectable to a first host unit, a second host unit and a device via serial advanced technology attachment (SATA) links, said switch comprising:**

a first SATA port for connection to the first host unit, the first SATA port including a first host task file responsive to commands sent by the first host unit;

a second SATA port for connection to the second host unit, the second SATA port including a second host task file responsive to commands sent by the second host unit;

a third parallel ATA (PATA) port for connection to the device, the third PATA port including a device task file, the device supports queuing of the

commands sent by the first and second host units and generates an original queue depth value indicative of a number of commands that the device can queue from either of the first or second host units; and

an arbitration and control circuit, coupled to said first host task file, to said second host task file, and to said device task file, for selecting one of the first or second host units to concurrently access the device through the switch, by accepting the commands from either of the first or second host units, at any given time, including when the device is not in an idle state, the arbitration and control circuit being responsive to the original queue depth value and alters the original queue depth value to be a new queue depth value that is less than the original queue depth value so that each of the first and second host units is assigned less than the number of commands indicated by the original queue depth value but that a total number of commands queued by the first and second host units remains the same as the original queue depth value thereby misrepresenting the original queue depth value to the first and second host units to be less than the original queue depth value thereby preventing the commands sent by the first and second host units from being lost by an overrun of the original queue depth value by either of the first or second host units ..." The prior art of record including the disclosures of Grieff et al. (US Patent 6,961,813), "SATA vs. PATA: the reality of Serial and Parallel ATA - Serial ATA", Utsunomiya et al. (US Pub.: 2003/0131166), Ooi et al. (US Patent 6,854,045) and Ooi et al. (US Patent 6,961,787) neither anticipates nor renders obvious the above recited combination. Because claims

32 and 36-43 depend directly or indirectly on claim 31, these claims are considered allowable for at least the same reasons noted above.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/C.K.L./

December 05, 2008

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

/Alford W. Kindred/

Supervisory Patent Examiner, Art Unit 2181